REMARKS

Claims 3, 4, 6-9, 11-17, 19-26, 55-62 and 75-79 are pending in this application. Applicant acknowledges, with appreciation, the Examiner's allowance of claims 6, 8, 9, 11, 12, 15-17, 19-26, 55-62 and 75-79. Claims 3, 4, 7, 13 and 14 stand rejected.

Claims 3, 4, 13 and 14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Applicant Admitted Prior Art ("AAPA").

In the statement of the rejection, the Examiner admitted that Yen does not teach all the limitations recited in claims 3, 4, 13 and 14. However, the Examiner applied Applicant's arguments as an admission of prior art that teaches the missing feature of Yen. This rejection is respectfully traversed.

Applicant submits that Yen does not disclose, among other things, that "at least one buffering circuit buffering said output clock signal such that a logic low period and a logic high period of said output clock signal are different from each other," recited in claims 3 and 4. Applicant also submits that Yen does not disclose, among other things, "at least one buffer circuit for changing a duty ratio of said output clock signal," recited in claims 13 and 14.

In the statement of the rejection, the Examiner asserted that Fig. 7B of Yen discloses the claimed buffering circuit configured to change a duty ratio of a clock signal. However, Applicant emphasizes that Yen does not have a function to change the duty ratio of the clock signal, although the reference appears to disclose a function to change the frequency of the clock signal.

In Figs. 7A and 7B of Yen, when the capacitive load of variable-load clock VLCLK changes in response to first and second control signal CTL1, CTL2, this change affects both rising and falling edges of fixed-frequency clock FCLK according to the following two reasons (i) and (ii).

(i) Control signal CTL1, CTL2 are synchronous with the rising edge of fixed clock FCLK. Therefore, control signals CTL1, CTL2 rise or fall only once in cycle of fixed clock FCLK.

(ii) When the capacitive load of variable-load clock VLCLK changes, this change influences both charging (rising) and discharging (falling) of buffer (VLCLK driver) 22. See, e.g., Fig. 3 and relevant description of Yen.

Accordingly, Yen cannot control both rising and falling edges of a clock signal. As a result, Yen is not capable of changing the duty ratio of a clock signal by using the circuit shown in Fig. 7A.

In Fig. 7B of Yen, the duty ratio of modulated clock MCLK differs between the second and fourth pulses. This is so because the delay of modulated clock MCLK changes in the timing of the second and fourth pulses. Due to this delay change, an initial pulse of MCLK varies in shape. This phenomenon is occurred in delay change.

The above change of duty ratio in Fig. 7B, however, occurs only in the moment of an initial pulse when the delay of modulated clock MCLK changes in the timing of the second and fourth pulses. This is quite different from the claimed invention in which a buffer circuit continuously buffers a clock signal with changed duty cycle.

If control signals CTL1, CTL2 of Fig. 7B vary in every cycle of fixed clock FCLK, the duty ratio could be changed in every cycle. Even in that case, however, when one "H" period is extended in Fig. 7B, the next "H" period must be narrowed. This is quite different from the claimed invention in which the buffer circuit buffers a clock signal with changed duty ratio to continuously maintain the duty ratio.

From another point of view, the phase of rising edge between fixed clock FCLK and modulated clock MCLK could be changed in Yen. In the claimed invention, however, the phase of rising edge between a source clock (corresponding to FCLK) and an output clock (corresponding to MCLK) could not be changed.

Due to the above changed phase, a clock generation circuit of the claimed invention can synchronize data transmission among modules under different duty control. The claimed invention can also synchronize data transmission from an external interface of an LSI. In contrast, Yen cannot synchronize data transmission among modules operated by different clocks. Therefore, another device such as an interface for asynchronous operation is additionally required to Yen, which cause the increase of circuits.

It is submitted that there is no prior art teaching that would have compelled an artisan to modify the Yen arrangement to meet all the limitations recited in claims 3, 4, 13 and 14. It is, thus, submitted that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for at least lack of the requisite factual basis. Applicant, therefore, solits withdrawal of the imposed rejection of claims 3, 4, 13 and 14 under 35 U.S.C. §103 for obviousness predicated upon Yen in view of the AAPA.

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Suda.

In the statement of the rejection, the Examiner admitted that Yen does not teach the frequency-multiplied circuit as recited in claim 7. However, the Examiner applied Suda and asserted that the reference teaches the missing features of Yen. The Examiner then concluded that it would have been obvious to modify Yen's device based on the teachings of Suda to arrive at the claimed invention. This rejection is respectfully traversed.

Applicant specifically submits that Yen and Suda, either individually or in combination, do not teach a clock generation circuit, among other things, "a buffer portion buffering said output clock signal," and "said output clock signal having a logic high period and a logic low period different from each other," as recited in claim 7.

As discussed above with respect to the rejection of claims 3, 4, 13 and 14, Yen does not teach changing a duty ratio of a clock signal. Claim 7 recites, among other things, "a buffer portion buffering said output clock signal," and "said output clock signal having a logic high period and a logic low period different from each other."

Accordingly, the applied combination of Yen and Suda does not teach all the limitations recited in claim 7. It is, thus, submitted that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for at least lack of the requisite factual basis. Applicant, therefore, submits that the imposed rejection of claim 7 under 35 U.S.C. §103 for obviousness predicated upon Yen in view of Suda is not viable and, hence, respectfully solicits withdrawal thereof.

Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Tomoki Tanida

Tomoki Tanida
Limited Recognition No. L0098

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 SAB:TT
Facsimile: 202.756.8087
Date: May 11, 2006

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